TERMINATION STRUCTURE OF DMOS DEVICE

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims priority from R.O.C. Patent Application No. 092107170, filed Mar. 28, 2003, the entire disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a termination structure and more particularly to a termination structure applied to trenched DMOS devices.

The DMOS (diffused MOS) device is an important power transistor widely used in high voltage systems such as power suppliers, power control devices, etc. Among many known structures of power transistors, a trenched power transistor is a notable design. Some reports note that trenched MOSFETs have better improvement than planar power MOSFETs in efficiency and integration.

FIG. **1**A through FIG. **1**F depict a sequence of steps to form a typical trenched DMOS device. In FIG. **1**A, an N-type epitaxial layer **10** is formed on an N+ silicon substrate **1**. A thermal oxidation process is then performed to grow an initial oxide layer **20** over a location of a termination structure. By using the initial oxide layer **20** as a mask, P-type dopants are implanted to form a P-type active area **12** in the epitaxial layer **10**. In FIG. **1**B, a plurality of DMOS trenches **13** extending from the P-type active area **12** to the epitaxial layer **10** below the P-type active area **12** is formed by etching. Afterward, an oxidation process is performed to form a gate oxide layer **21** over the P-type active area **12** and to make the initial oxide layer **20** become a field oxide layer **22**. In FIG. **1**C, a polysilicon layer is deposited by a chemical vapor depositing (CVD) process. The portion of the polysilicon layer on the surface of the epi layer **10** and outside the DMOS trenches is removed by etching, so that a plurality of poly gates **30** is formed respectively in the DMOS trenches **13**. Afterward, as shown in FIG. **1**D, a lithographic process is carried out to define a location of source regions **40** and to form a photoresist layer **40**PR as a mask. N-type dopants are implanted into the active area **12** to form N+ source regions **40** surrounding the DMOS trenches **13**. In FIG. **1**E, an isolation layer **50** is formed. An etching process is performed to form a plurality of contact windows **51** of the active area over the N+ source regions **40**. P-type dopants are implanted to form P+ regions **41** surrounding the N+ source regions **40**. As shown in FIG. **1**F, a metal contact layer **60** of the source regions is then deposited over the isolation layer **50**. The metal contact layer **60** contacts the P-type active area **12** through the contact windows **51**. The metal contact layer **60** has an opening over the field oxide layer **22** to expose the isolation layer **50**. In addition, a metal contact layer **61** of drain regions is formed on the backside of the N+ silicon substrate **1**. A driving voltage can be applied to the metal contact layer **61** and **60**, while a control voltage is applied to the polysilicon gate **30** to decide whether the source region and drain region of the DMOS are conductive with each other.

Although trenched power transistors are better than planar ones, the process for forming a trenched power transistor needs more lithographic processes because a trenched power transistor has a more complex structure than a planar one. It is desirable to provide an improved process for forming trenched power transistors.

In addition, because the power transistor devices usually bear a high voltage, a termination structure is necessary for preventing electric breakdown from early happening. There are several conventional termination structures widely used, such as a local oxidation of silicon (LOCOS), a field plate, and a guard ring, etc., among which the LOCOS is the simplest. As shown in FIG. **1**F, a termination structure of a field oxide layer **22** is at the right side of the figure. The thickness of the field oxide layer **22** can reach hundreds of nanometers. To form the field oxide layer **22**, a special mask for the active area is needed in the process. As shown in FIG. **1**A, the initial oxide layer **20** is formed through the active area mask. Then, the initial oxide layer **20** is thermally grown to be the field oxide layer **22**.

Moreover, it is for the field oxide layer **22** as the main portion of a termination structure. As shown in FIG. **1**A, after the formation of the initial oxide layer **20**, an ion implantation process of P-type dopants is performed by using the initial oxide layer **20** as a mask to form a P-type active area **12**. Therefore, the dopant concentration of the P-type active area **12** cannot be homogeneous. It impacts on the electric properties of the edge of the P-type active area and makes the device design more difficult. A cylindrical type of the P-N junction would be formed at the edge of the P-type active area **12**, so as to make the current more dense. Therefore, it causes electric breakdown to happen easily.

Due to the process characteristics of the LOCOS method, the field oxide layer **22** has a bird beak structure penetrating into the neighboring P-type active area **12**. Not only does it affect the precision of the transistor device dimension, but also causes electric field crowding in the neighborhood. This results in the increase of leakage current and decline of the performance of the active area.

In order to solve the above problem, there have been some designs proposed. FIG. **2**, depicts a conventional DMOS device and its termination structure, as described in U.S. Pat. No. 6,309,929. The '929 patent uses an epitaxial layer to form an active area **12** of the DMOS device and also uses a first trench **14** as the main portion of the termination structure. Afterward, a gate oxide layer **21** and a polysilicon layer are subsequently formed (not shown). The polysilicon re-fills the first trench **14** and a plurality of DMOS trenches **13**. Without a lithographic process, the redundant polysilicon layer is removed by an etchback in order to form a plurality of polysilicon gates **30** and a polysilicon sidewall **33** of the first trench **14**. Afterward, the exposed gate oxide layer **21** is removed, and then a dielectric oxide layer **53** is deposited. Without a lithographic process, the redundant dielectric oxide layer **53** is removed by an etchback process in order to make the dielectric oxide layer cover the surface of the polysilicon gates **30** and the polysilicon sidewall **33**. Thereafter, a TEOS layer **54** is deposited and then processed by the lithographic and etching processes to define the source regions **40**. Afterward, a source metal layer **60** is deposited. Through a lithographic and etching process, the source metal layer **60** only covers the P-type active area **12** and extends toward the termination structure by a certain distance.

The '929 patent can eliminate the lithographic processes applied to the polysilicon layer and used to form the field oxide layer **22**. However, due to the process characteristics, the thickness of the dielectric oxide layer **53** is limited, so that it affects the efficiency of the isolation between the polysilicon gate and the source metal contact layer.

In addition, for the power transistor design, to prevent the effect of electrostatic discharge, an ESD (electrostatic discharge) device **16** is introduced as a protective method. As